PPG

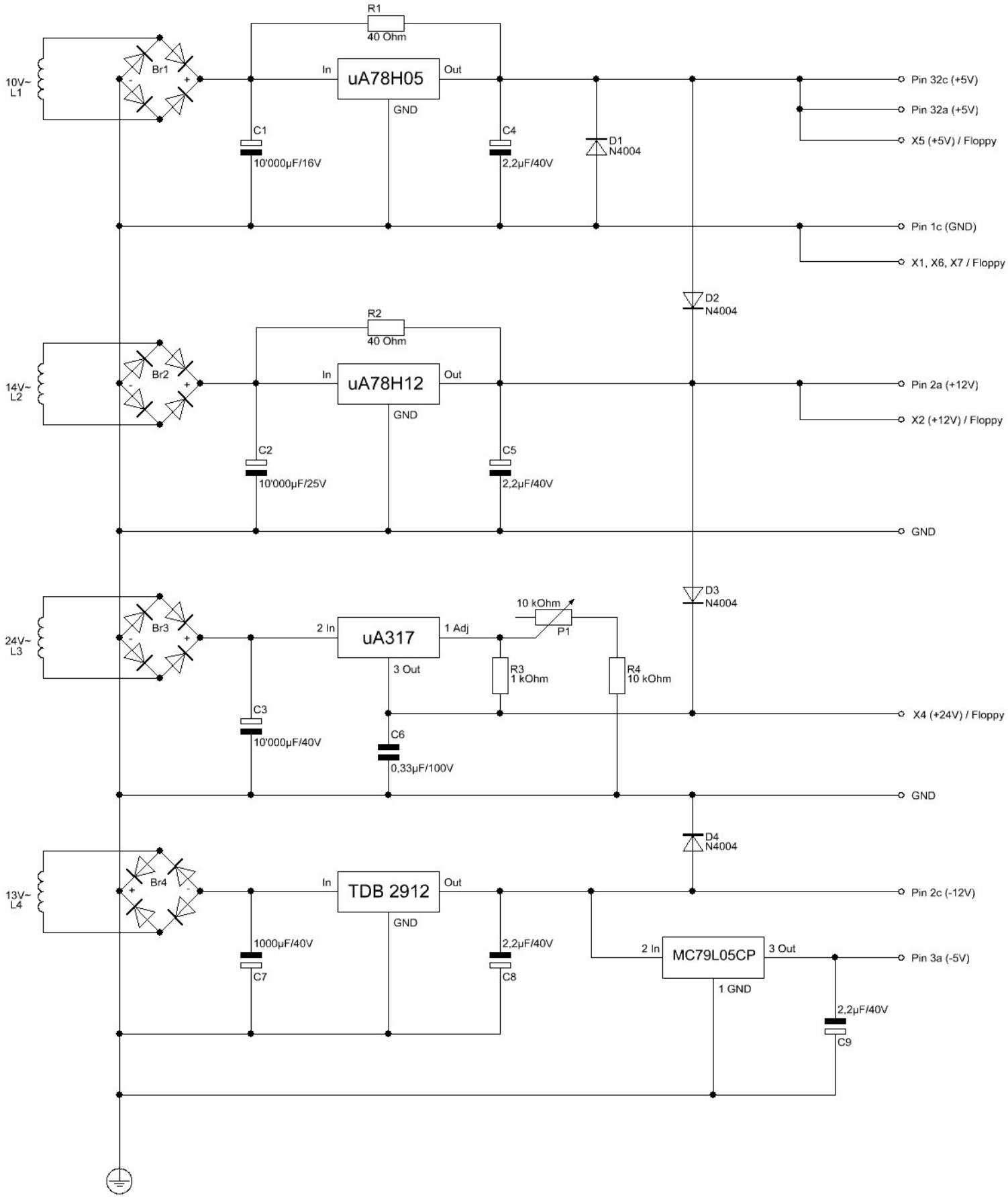
waveterm

Service Manual

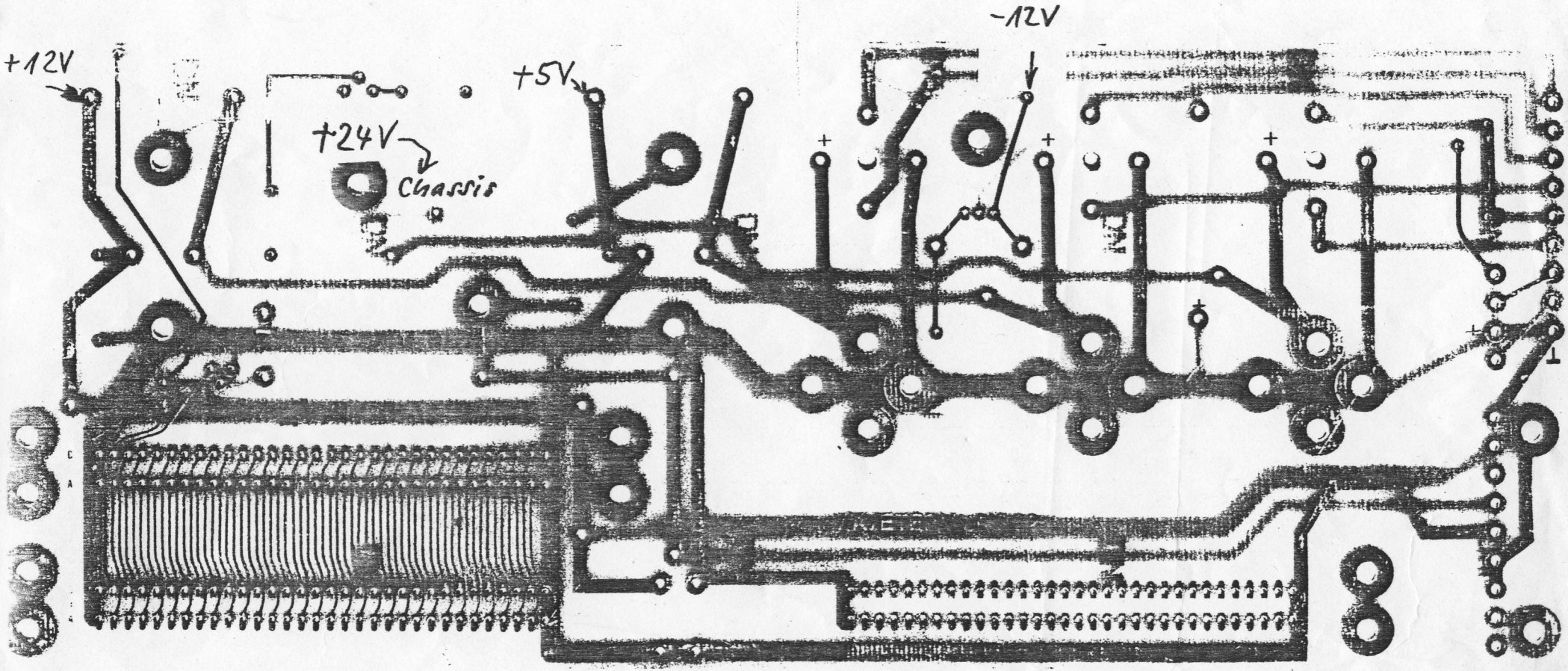
PPG Waveterm A (PSU)

v 0.3

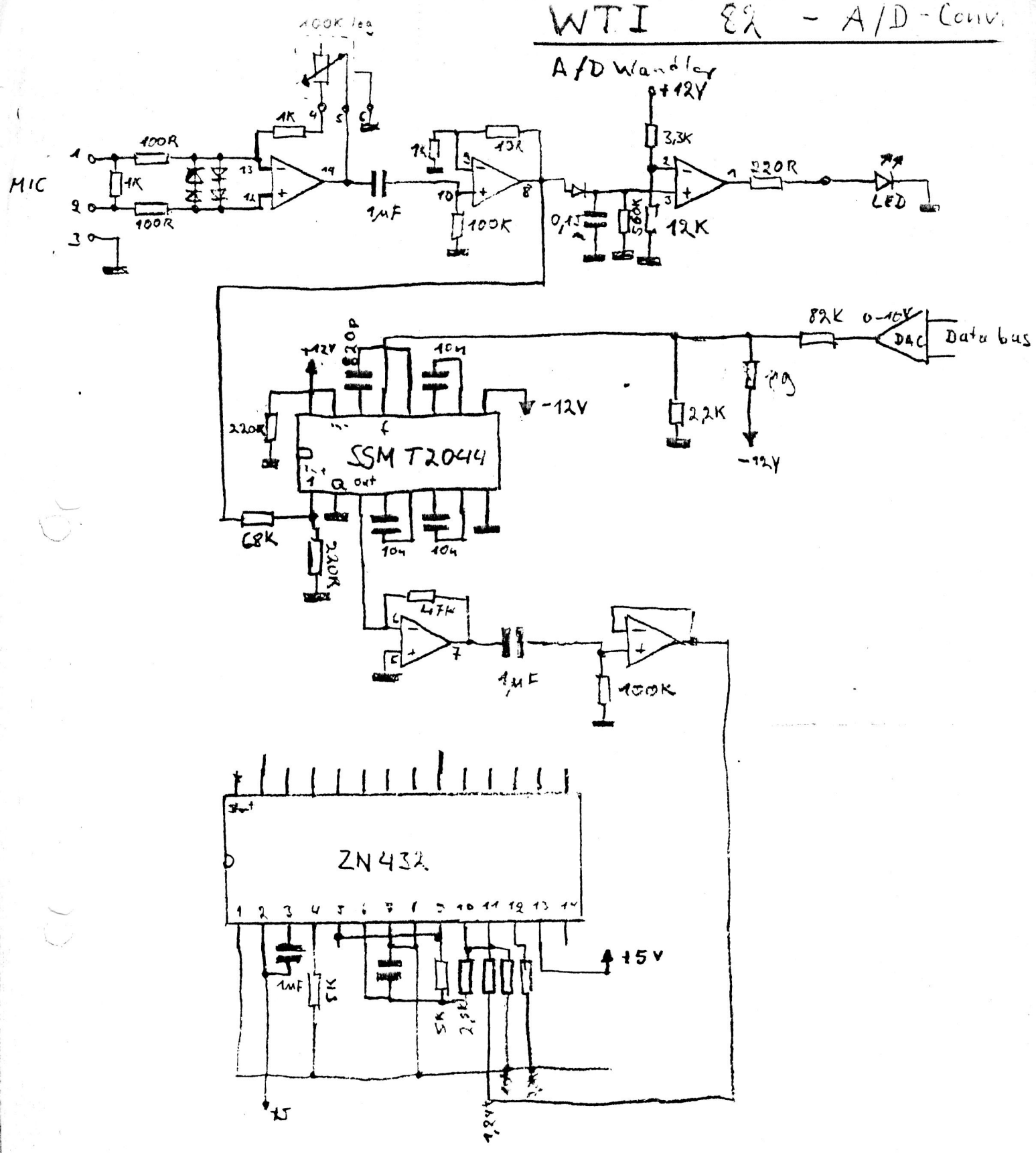
Input 230V~/50Hz

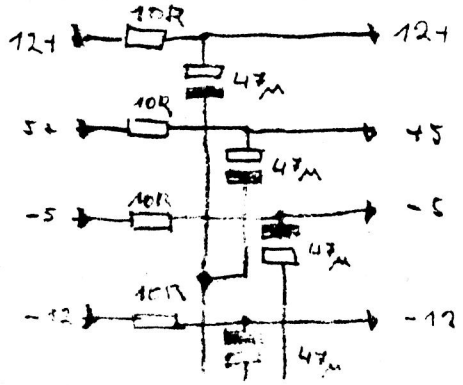


WAVE - TERM Power Suply



WTI 82 - A/D-Conv.





FERRANTI semiconductors

A to D CONVERTER

ZN432 Series

10-Bit Successive Approximation Monolithic A/D Converter

FEATURES

- 10, 9 and 8-Bit Accuracies
- 3 Operating Temperature Ranges
- 20 μs Conversion Time Guaranteed
- Input Range as Desired
- ±5V Supplies, TTL/CMOS Compatible
- Parallel and Serial Outputs
- Bipolar Monolithic Construction

DESCRIPTION

The ZN432 range of successive approximation analogue to digital converters combine several innovations to provide this function on a fully monolithic silicon integrated circuit. The chip contains a current switching array using a matrix of diffused resistors (no trim required), successive approximation logic with TTL interfacing, 2.5V precision voltage reference with reference amplifier, and fast comparator with good overload recovery. The overall accuracy of the A-D system is sufficient to provide guaranteed monotonicity over the operating temperature range.

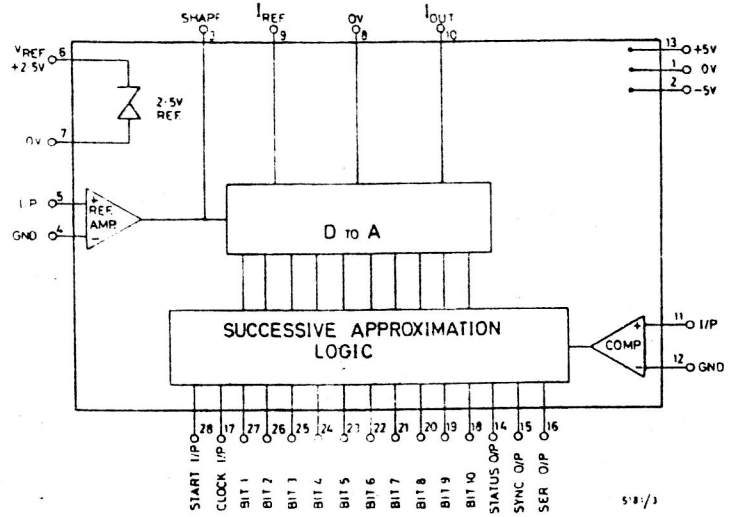


Fig. 1 – INTEGRATED CIRCUIT BLOCK DIAGRAM

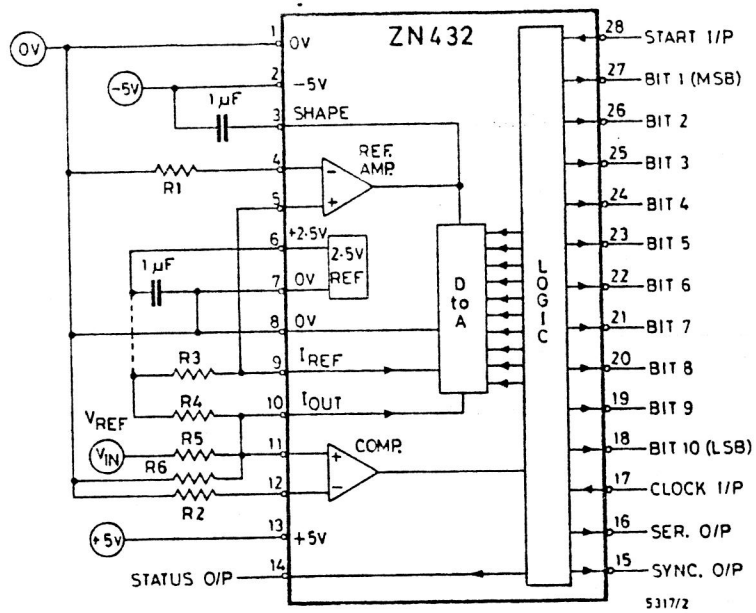
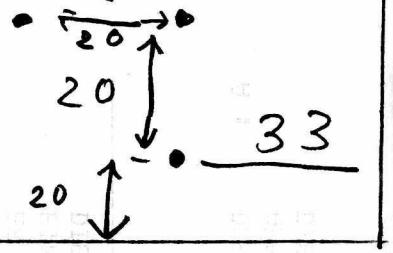


Fig. 2 – TYPICAL EXTERNAL COMPONENTS

ORDERING INFORMATION

Operating Temperature	10-bit accuracy	9-bit accuracy	8-bit accuracy	Package
–55 to +125°C	ZN432J-10	ZN432J-9	ZN432J-8	Ceramic
–40 to +85°C	ZN432BJ-10	ZN432BJ-9	ZN432BJ-8	Ceramic
0 to +70°C	ZN432CJ-10	ZN432CJ-9	ZN432CJ-8	Ceramic



ASK-MAN2

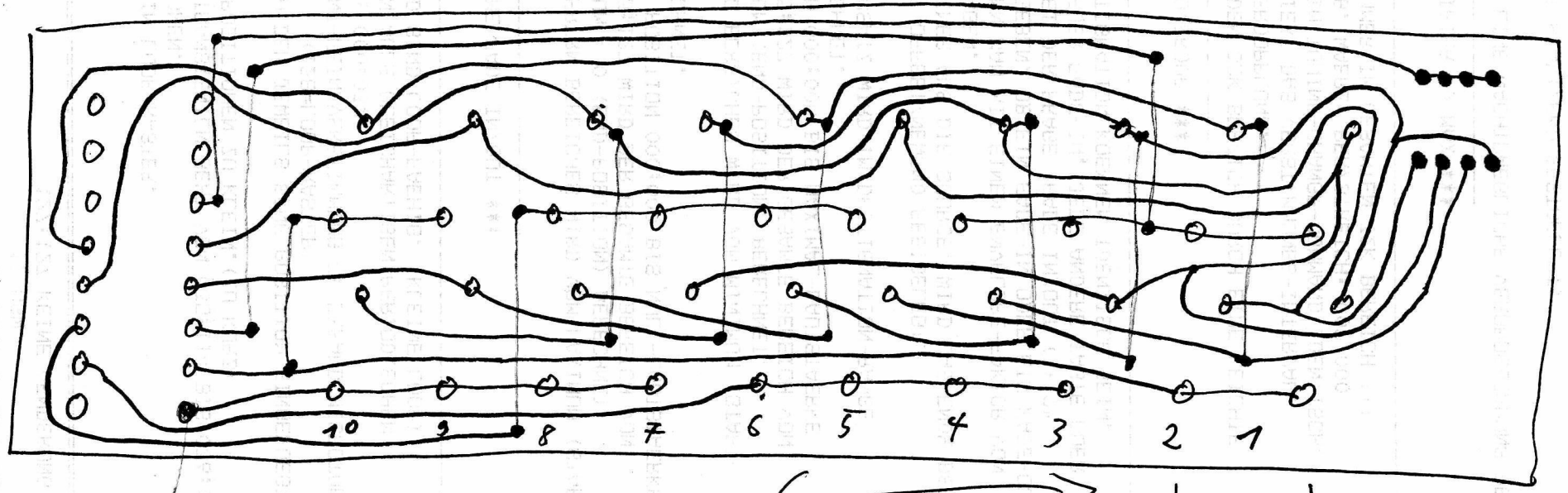
MAC2

ASK-WT

11 Leitungen

Lötseite!

Soft Keys



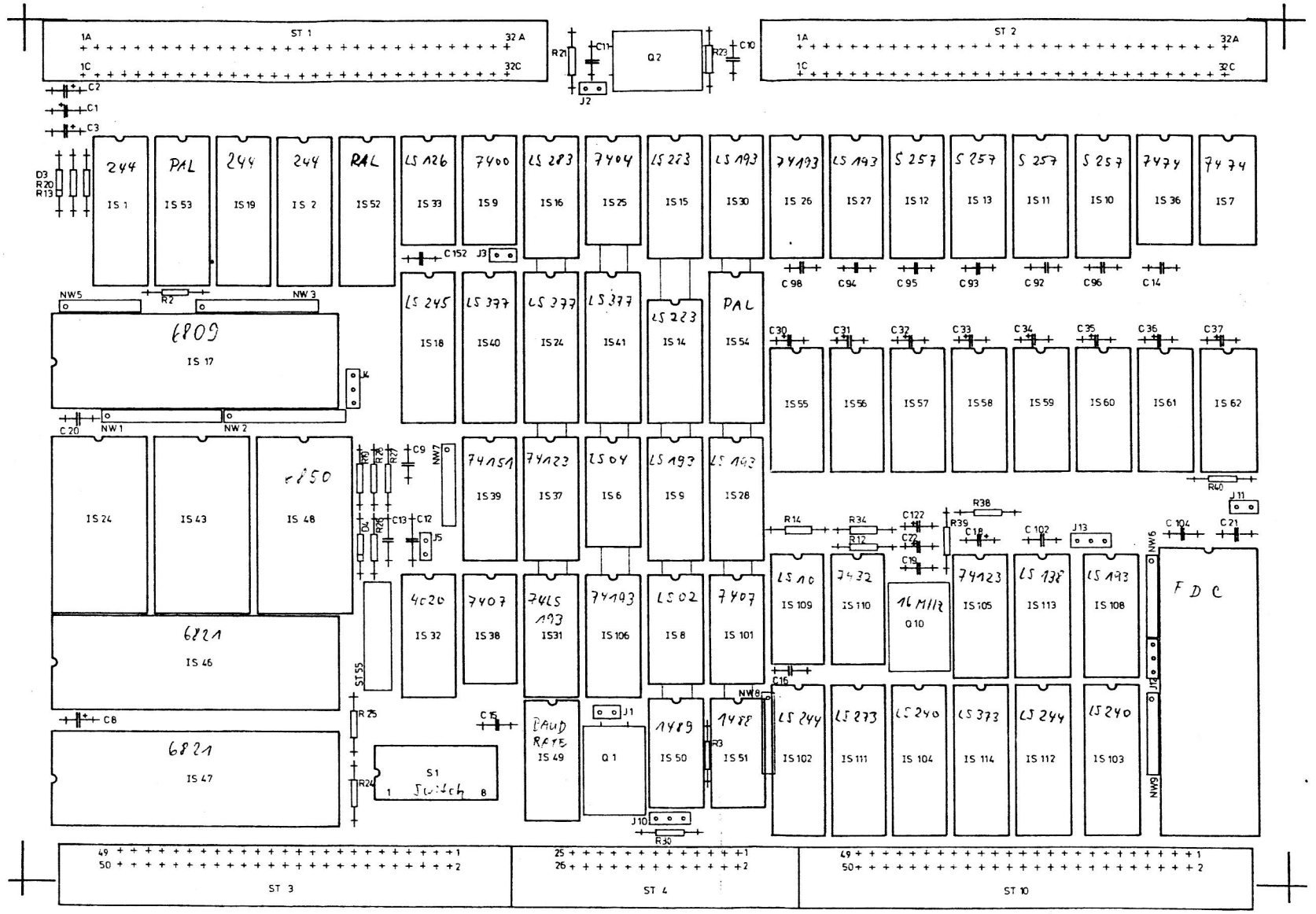
Flachkabel

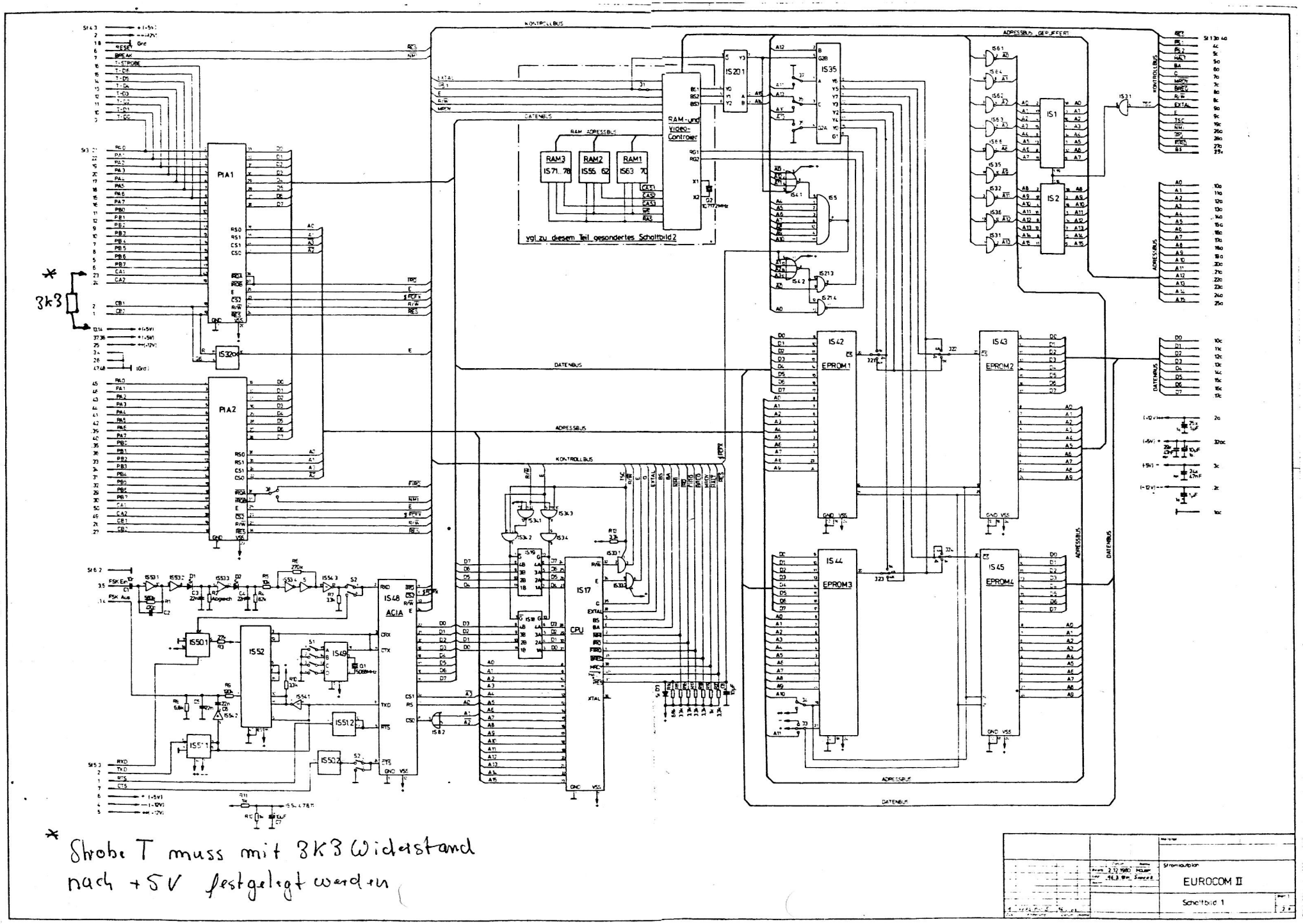
Flachkabel weiter Anschluß

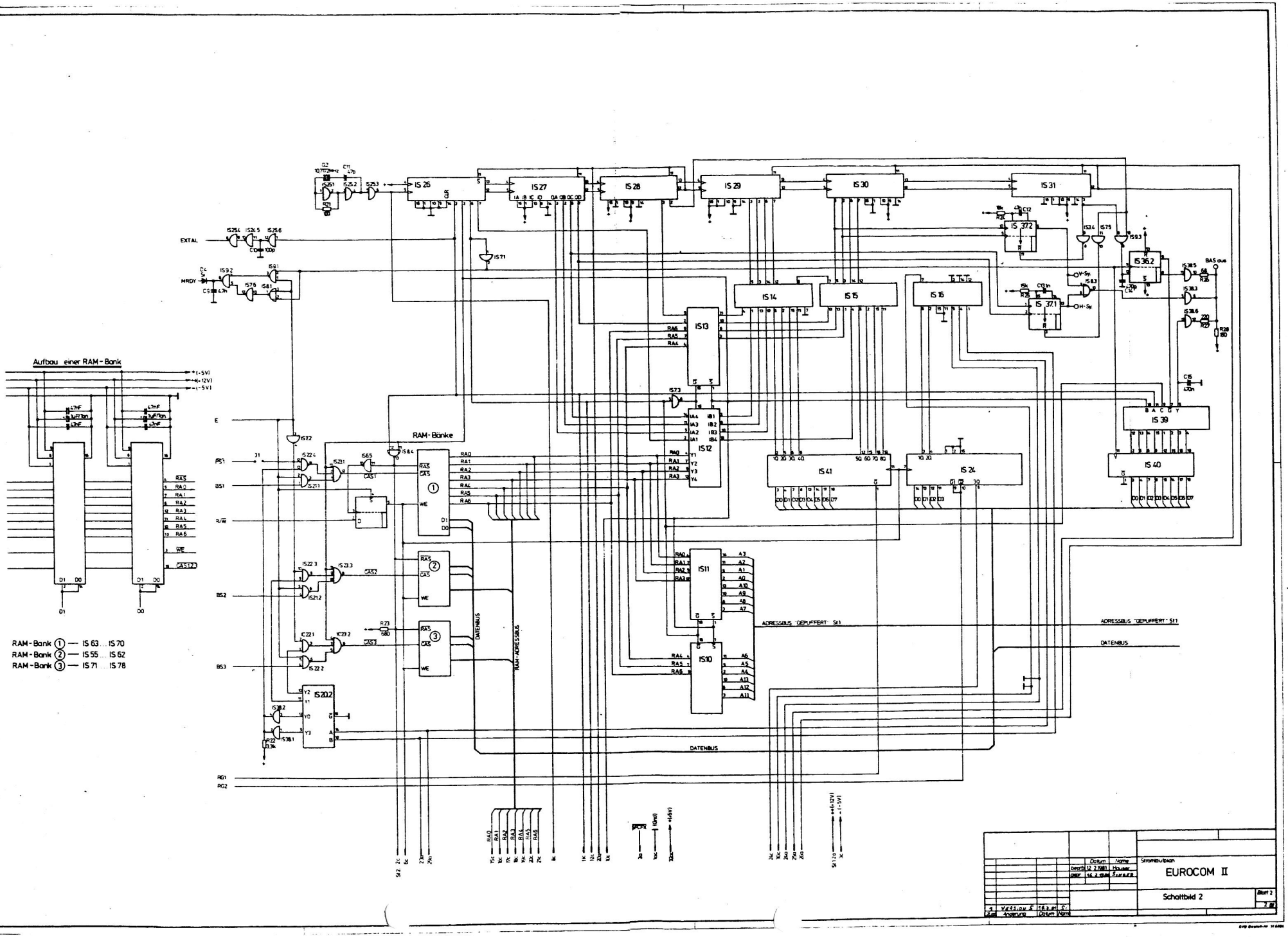
ext. Pia

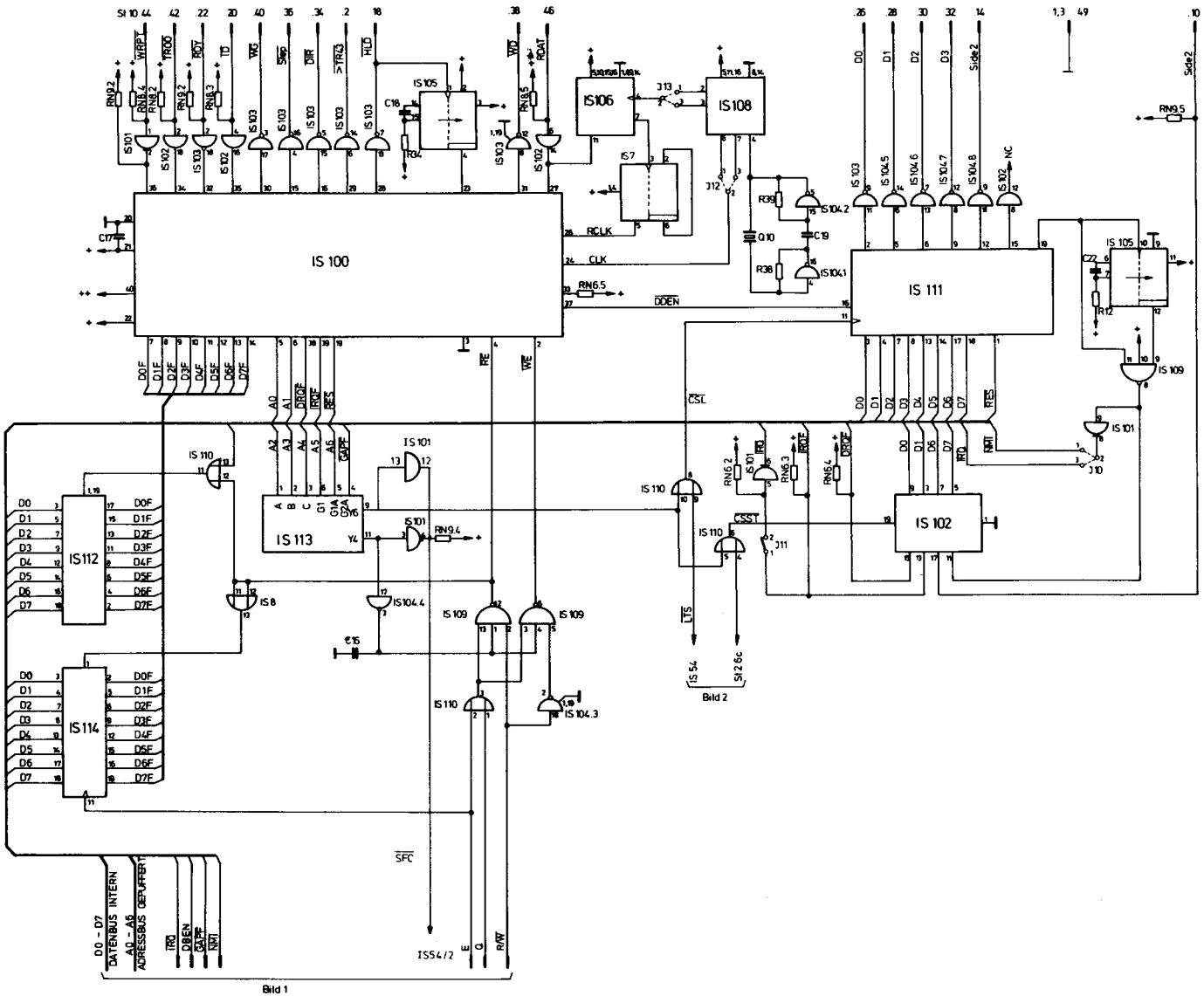
Pin 26

Wavetek 77 A


ST 1
1A
32 A
1C
32C
ST 2
1A
32A
1C
32C
R21
C11
Q2
R23
C10
J2
C2
C1
C3
D3
R20
R13
244
IS 1
PAL
IS 53
244
IS 19
244
IS 2
RAL
IS 52
LS 126
IS 33
7400
IS 9
LS 283
IS 16
7404
IS 25
LS 253
IS 15
LS 193
IS 30
74193
IS 26
LS 193
IS 27
S 257
IS 12
S 257
IS 13
S 257
IS 11
S 257
IS 10
7474
IS 36
74 74
IS 7
C 152
J3
C 98
C 94
C 95
C 93
C 92
C 96
C 14
NW5
R2
NW 3
6809
IS 17
J4
C 20
NW 1
NW 2
LS 245
IS 18
LS 377
IS 40
LS 377
IS 24
LS 377
IS 41
LS 223
IS 14
PAL
IS 54
C30
C31
C32
C33
C34
C35
C36
C37
IS 55
IS 56
IS 57
IS 58
IS 59
IS 60
IS 61
IS 62
R40
J11
IS 24
IS 43
8250
IS 48
R30
R31
R32
R33
C9
NW7
D4
R26
C13
C12
J5
74151
IS 39
74123
IS 37
LS 04
IS 6
LS 193
IS 9
LS 193
IS 28
R14
R34
R12
C122
C7
C19
R38
R39
C18
C102
J13
C 104
C 21
NW6
LS 10
IS 109
7432
IS 110
16 MHz
Q 10
74123
IS 105
LS 138
IS 113
LS 193
IS 108
F D C
J12
NW9
6821
IS 46
4020
IS 32
7407
IS 38
74LS 193
IS31
74193
IS 106
LS 02
IS 8
7407
IS 101
ST55
C16
NW8
LS 244
IS 102
LS 273
IS 111
LS 240
IS 104
LS 373
IS 114
LS 244
IS 112
LS 240
IS 103
C8
6821
IS 47
R25
R24
S1
Switch
1
8
C15
BAUD RATE
IS 49
Q 1
J1
1489
IS 50
1488
IS 51
R3
J10
R30
49
50
ST 3
25
26
ST 4
49
50
ST 10
Maßstab
Datum
Name
Bearb.
8.4.88
BOMBAU
Gepr.
Norm
BESTÜCKUNGSPLAN
EUROCOM II V7
ELTEC
Blatt
Zust.
Änderung
Datum
Name

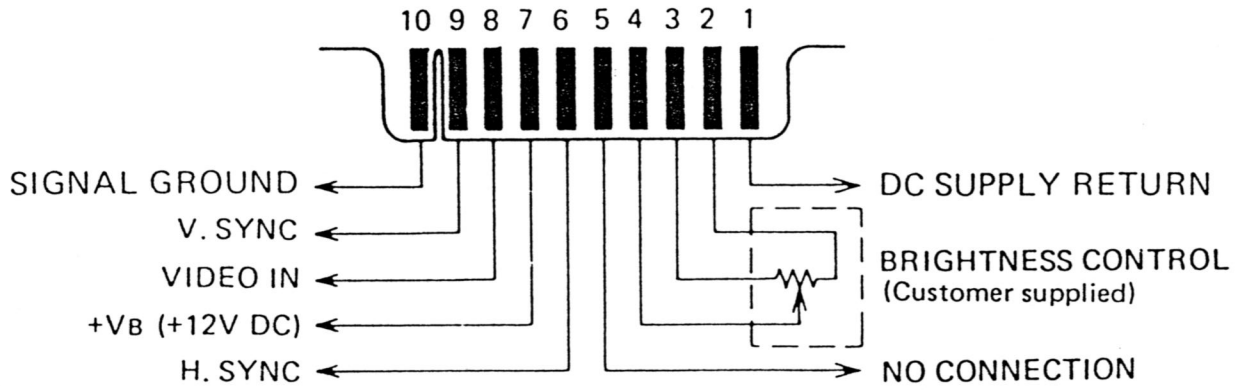

KONTROLLBUS
ADRESSBUS GEPUFFERT
DATENBUS
RAM ADRESSBUS
RAM-und Video-Controler
RAM3 IS71..78
RAM2 IS55..62
RAM1 IS63..70
vgl. zu diesem Teil gesonderter Schaltbild 2
PIA1
PIA2
ACIA
CPU
EPROM1
EPROM2
EPROM3
EPROM4
3k3
* Strobe T muss mit 3K3 Widerstand nach +5V festgelegt werden
EUROCOM II
Schaltbild 1


Aufbau einer RAM-Bank
RAM-Bänke
RAM-Bank ① — IS 63 ... IS 70
RAM-Bank ② — IS 55 ... IS 62
RAM-Bank ③ — IS 71 ... IS 78
ADRESSBUS "GEPUFFERT" S11
DATENBUS
RAM-ADRESSBUS
EXTAL
MRDY
E
RW
RG1
RG2
EUROCOM II
Schaltbild 2
Blatt 2



					DATUM	NAME	Stromlaufplan
				BEARB	13.1.1982	I-Lauser	EUROCOM II
				GEPR			Version 7
				NORM			
				ELTEC			Schaltbild 3
ZUST.	ÄNDERUNG	DATUM	NAME	Ersatz f.		Ers. d.	BLATT 3 / 3 BL

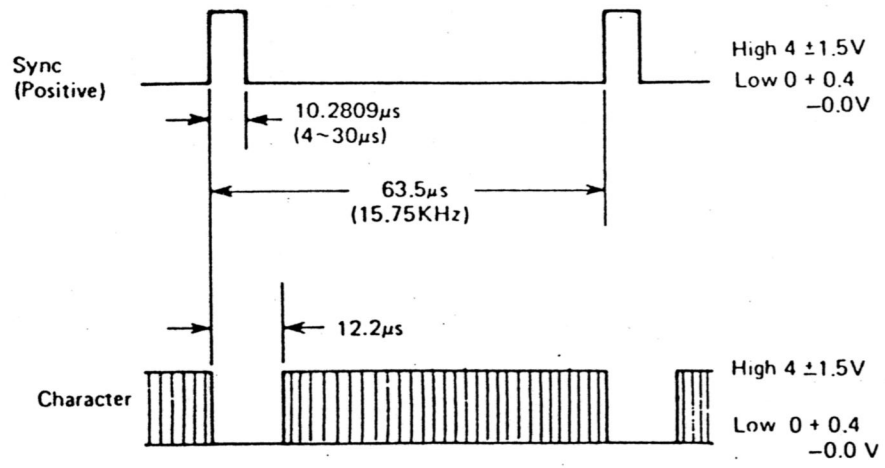
CONNECTOR WIRING



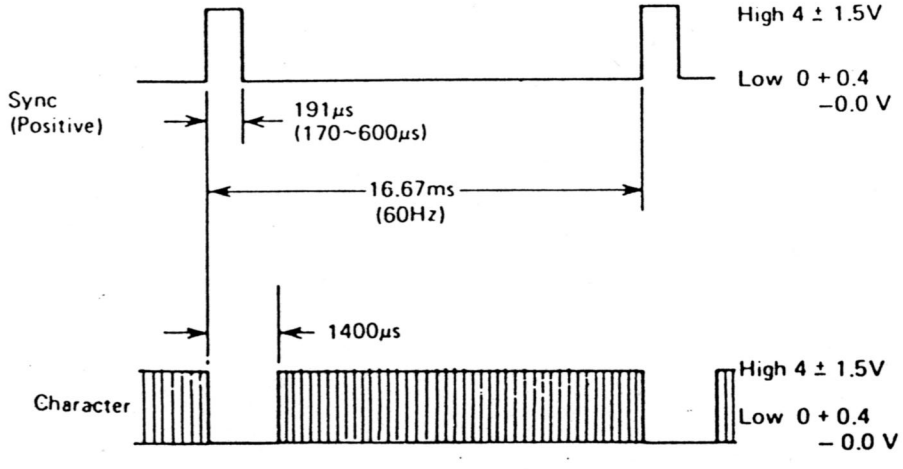
TIMING CHART

Note: Time Tolerance: ±0.1%
Sample unit is adjusted according to this timing and frequency.

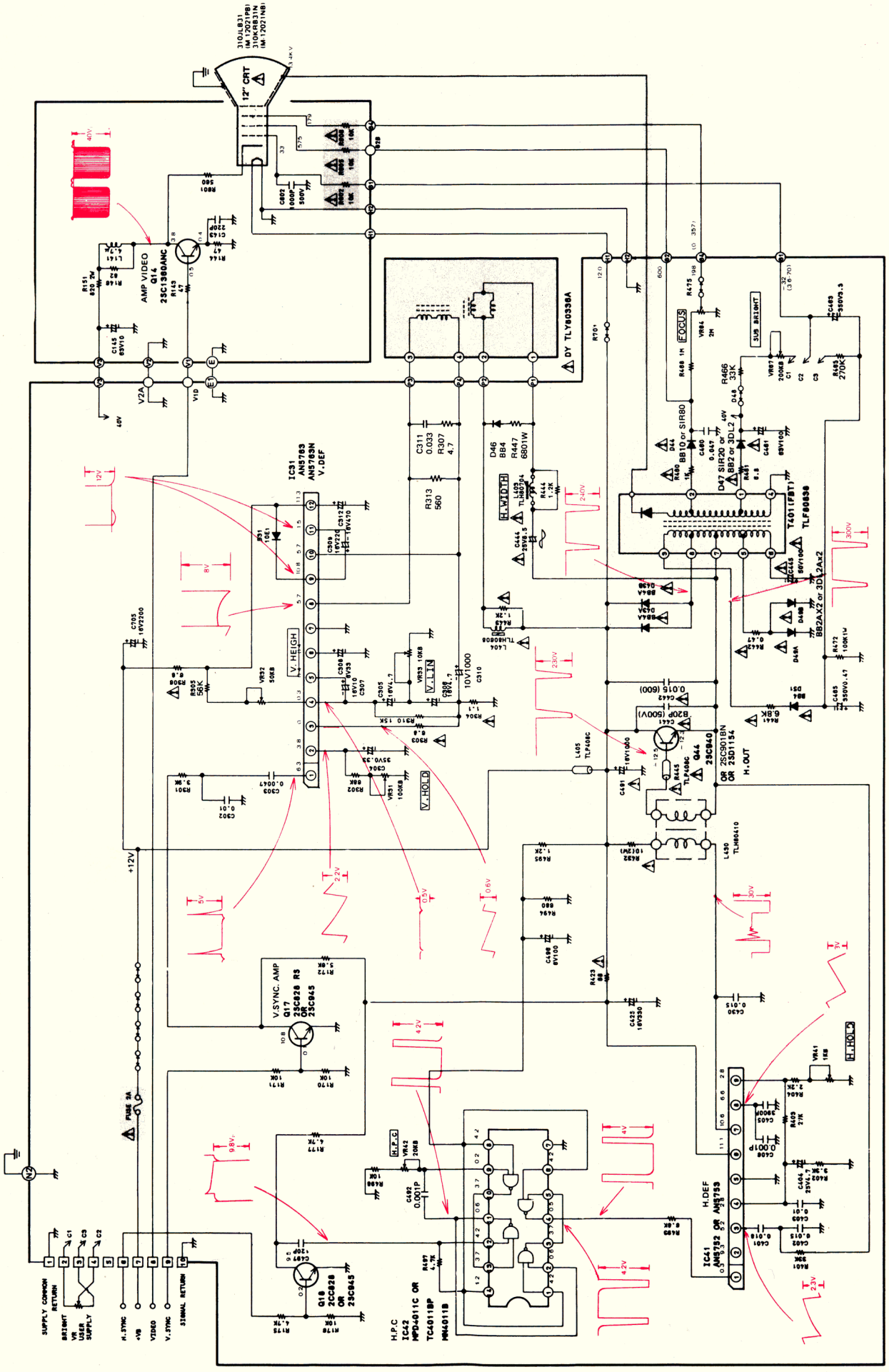
Horizontal Sync Timing



Vertical Sync Timing



SCHEMATIC DIAGRAM FOR MODELS M-12021PB/M-12021NB



INSTALLATION

2.1 MECHANICAL

Printed Wiring Assembly (PWA) for Monitor provides five mounting holes: one in each corner and one beside the heat sink. See Figure 1-1, BCX-200 Dimensions, for hole spacing data. Locate PWA so Fly-back Transformer, T101, has no conductive material closer than 3/8 inch.

2.2 ELECTRICAL

2.2.1 Input

PWA has one input connector, J106. It is a ten-contact, board-edge connector. Suggested mating connectors:

Viking 2VK10S/1-2
Amphenol 225-21031-101

Optional Mass Termination Connectors:

Molex 22-01-2107 with type No. 2759 contacts for discrete wires
Molex 22 26-8103 preloaded for mass termination

J106 contact identification:

1 - Horizontal Ground
2,3,4 - External Brightness Control, See Note 4, Figure 4-1, Functional Blocked Schematic
5 - Arc Ground
6 - Horizontal Drive
7 - +12 vdc
8 - Video
9 - Vertical Drive
10 - Video/Vertical Ground

2.2.2 Video

Video input line should be short as possible and separated from all other wiring.

2.2.3 Grounding

Video/Vertical Ground and Horizontal Ground are connected on the PWA. If desired, the two grounds can be separated by removing jumper wire W104, located about one inch from J106.

ALINEMENT

3.1 ALINEMENT

Monitor is factory alined and should not require any further adjustment. Following information is provided for future reference.

3.1.1 Horizontal Hold

a. Disconnect Horizontal Drive (sync) signal.
b. Set HORIZ HOLD (R149) to almost stop horizontal roll. Direction of adjustment not important.
c. Connect Horizontal Drive signal.

3.1.2 Vertical Hold

d. Adjust VERT HOLD (R105) clockwise to point where picture begins to roll down.
e. Set VERT HOLD counter-clockwise about 1/8 turn.

3.1.3 Raster Centering

f. Set ring magnets on rear of yoke to center raster.

3.1.4 Video Centering

g. Set HORIZ CENT (R138) for centering of video.

3.1.5 Brightness

h. Set BRT (R105) at point where raster just disappears.

3.1.6 Contrast

i. Using window signal, Set CTRS (R119) for rated light level.

3.1.7 Vertical Linearity

j. Set VERT LIN (R109) so characters in top and bottom rows have equal height.

3.1.8 Vertical Height

k. Set HEIGHT (R107) for required height.

3.1.9 Horizontal Linearity and Width

l. Adjust LINEARITY (L103) for maximum width.
m. Roughly adjust LINEARITY for best overall linearity. Maintain as much width as possible.
n. Roughly adjust WIDTH (L104) for desired width.
o. Set LINEARITY for best overall linearity.
p. Set WIDTH for desired width.

3.1.10 Focus

q. Set FOCUS (R162) for best compromise between best corner focus and best center focus.

THEORY OF OPERATION

Theory of operation is given by proper use of Figure 4-1, Functional Blocked Schematic, and Figure 4-2, Functional Blocked Theory.

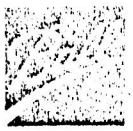
4.1 FUNCTIONAL BLOCKED SCHEMATIC

Schematic is blocked into 13 first level blocks such as VERTICAL DRIVE, HORIZONTAL DRIVE, etc. First level blocks are indicated by the lightest color blue background. Most first level blocks contain second level blocks indicated by darker blue background. For example, HORIZONTAL DEFLECTION contains two second level blocks: DT-1 and CS-1. One first level block contains second and third level blocks: HORIZONTAL DRIVE (first level, lightest blue) contains OSC-1 (second level, darker blue). OSC-1, in turn, contains MMV-1, CPS-2, FC-2, etc. These are all third level blocks and are indicated by darkest blue background. Note that every block is identified in the upper, left hand corner. Abbreviations used in second and third level blocks are identified in Functional Blocked Theory, Figure 4-2.

Gray shading indicates hardware and is used to identify PWA.

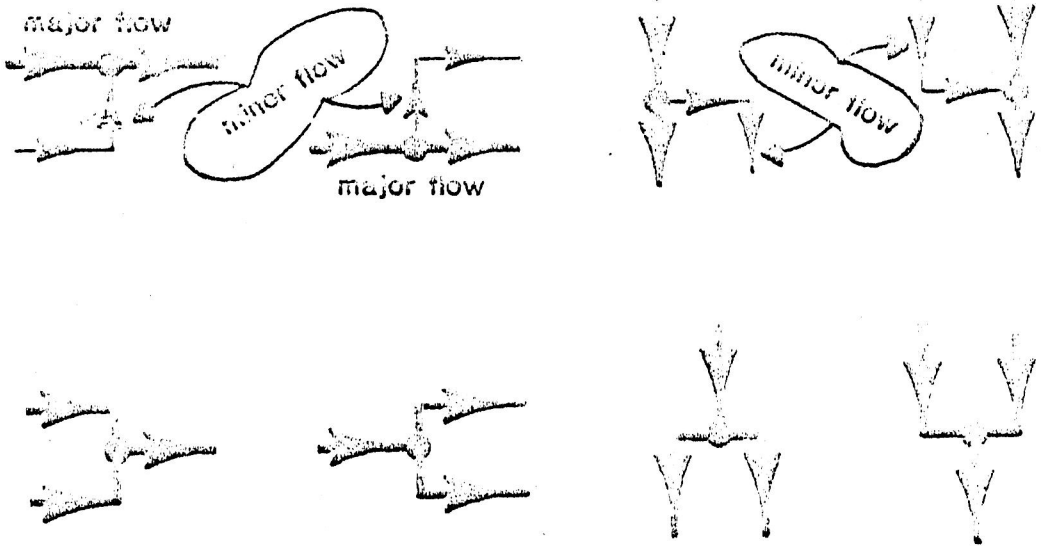
Schematic has been drawn, where practical, to following standards:

a. Signal flow is from left to right and is indicated by heavy lines and single arrowheads.
b. Minor signal flow (also left to right) is indicated by standard lines and single arrowheads.
c. Feedback signal flow is from right to left and is indicated by double arrowheads.
d. Voltages enter blocks at top and grounds leave blocks at bottom.
e. Inputs to blocks are at left and outputs at right.
f. Grounds are indicated by hollow triangles containing numbers. Numbers used correspond to jack pin numbers where grounds terminate. The exception to this is Arc Ground (J106-5) indicated by symbol.
g. Test points are located throughout schematic and are indicated by a hollow triangle containing TP and identifying numbers. Below schematic are test point location guides. These are grouped by function and located so schematic and location guide triangles point at each other as though connected by a straight vertical line. Test point guide intent is to make it easier to correlate test point physical locations in Figure 5-2, Test Point Locations, with schematic locations.
h. Current probe test points are located at inputs to horizontal and vertical yokes. They are indicated by a hollow triangle containing CP and identifying number.
i. Information such as voltage levels and warnings are enclosed in boxes which point to area concerned.
j. Warnings and adjustment points are highlighted with a white background.
k. Signal flow direction has been given priority over hardware layout. Therefore, hardware was shaped to accomodate requirement that signal flow beshown left to right.



l. Lines do not cross unless connected. Those which would ordinarily cross are interrupted by broken-line symbols.

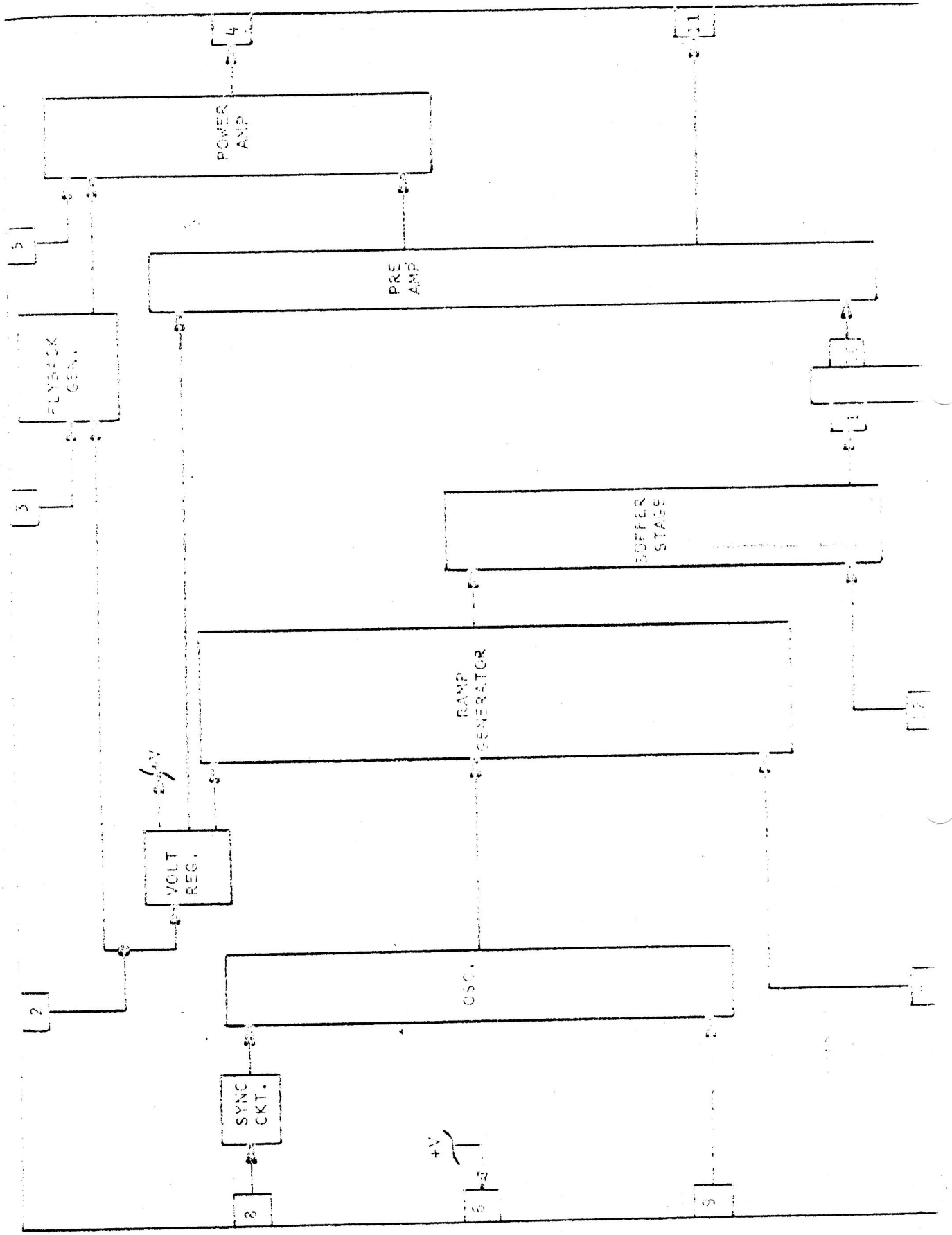
m. Power and signal flow lines are connected to show the order of importance as shown:



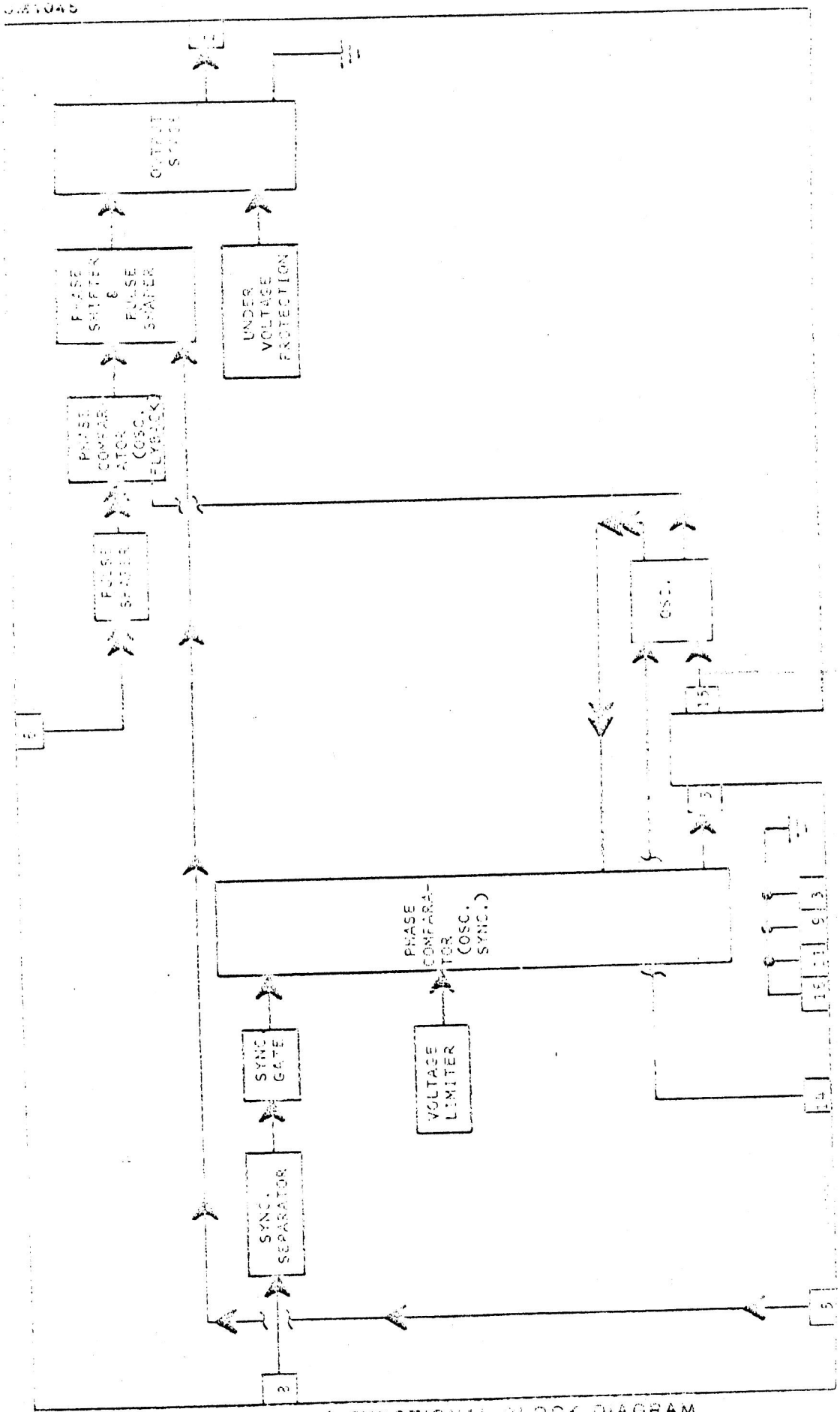
ALL LINES ARE MAJOR FLOW

4.2 FUNCTIONAL BLOCKED THEORY

Circuit theory is in functional blocked form. Background shading correspond to those used in the schematic. Text is for block in which it is contained.



U101 (IC-1) FUNCTIONAL BLOCK DIAGRAM



U102 (IC-2) FUNCTIONAL BLOCK DIAGRAM

FIGURE 4-4

TROUBLESHOOTING

This manual has been printed so the three major figures needed for troubleshooting can be viewed simultaneously:

a. Functional Blocked Schematic, Figure 4-1
b. Maintenance Dependency Chart, Figure 5-1
c. Test Point Location, Figure 5-2

	Maintenance Dependency Chart P/O Fig. 5-1	
Functional Blocked Schematic Fig. 4-1	Functional Blocked Theory Fig. 4-2 (Folded)	Signal Specification Table P/O Fig. 5-1
	Test Point Location Fig. 5-2	

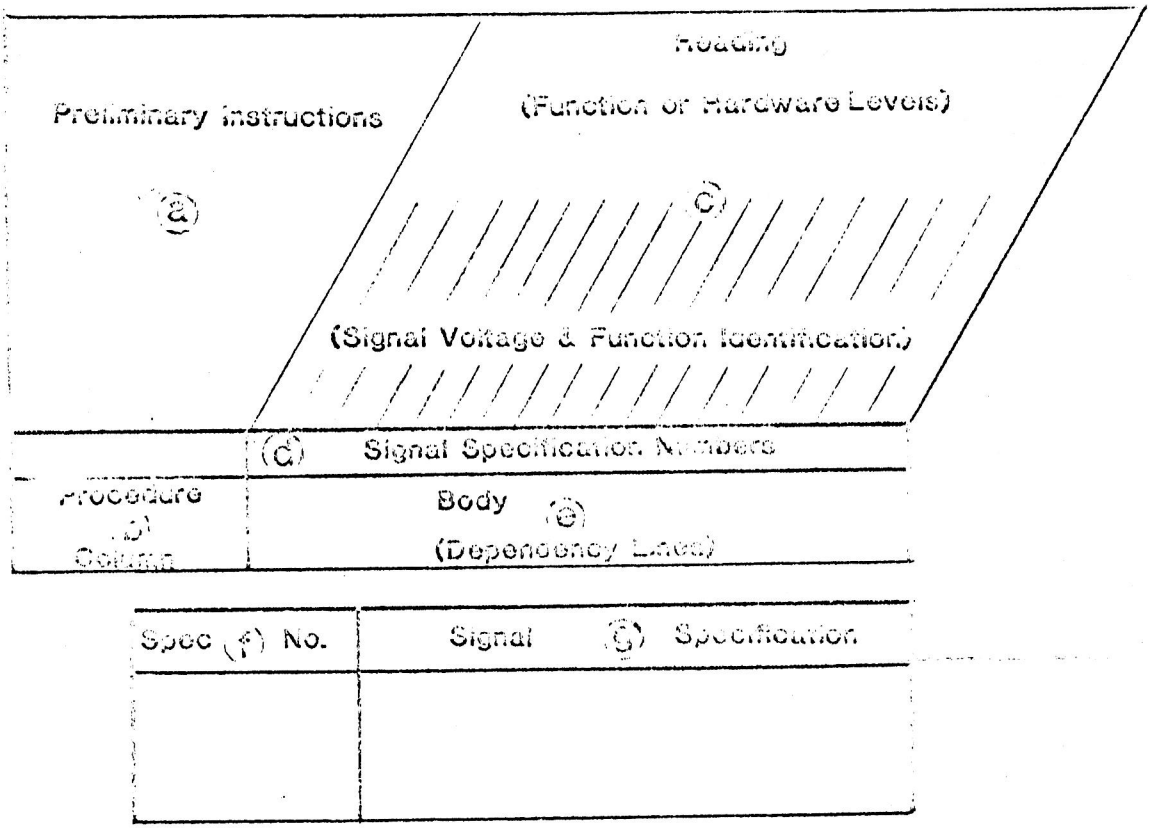
R157 +V on Time Bands, when
Anode CR107 TP 24 VR1
Pin 4 T104 TP 25
TPTP

Cross references between these figures are:

a. Test points (TP's) on schematic are referenced in the MDC and locations are grouped by function in Test Point Location.
b. Functional blocks and TP's on the schematic are referenced in the MDC.
c. Signal Specification (SS) numbers in the MDC are referenced for location in Test Point Location.

TP's were selected and associated data are given for a Monitor which is functioning properly. SS numbers were assigned and the related data are given for a faulty Monitor which is being tested.

MDC contains seven sections:



Four basic symbols are used in the Body, section e, to represent inputs, outputs, functions and their relationships:

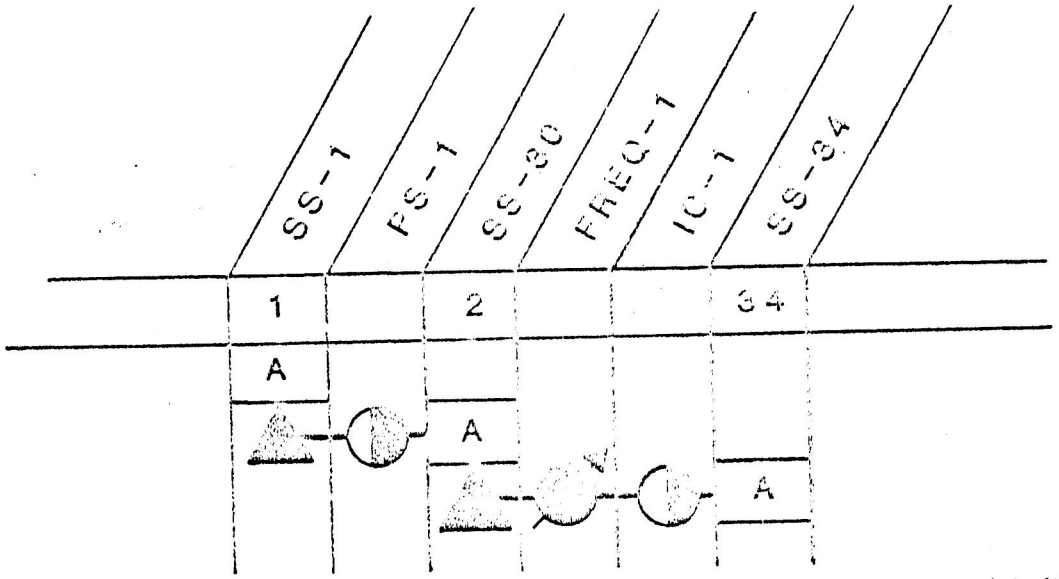
a. Box: represents input/output signals or voltages. The A in the box stands for "available", which means the signal or voltage is present and within specification. Each signal and voltage is assigned a number in section d. These numbers are repeated in section f and their specifications noted in section g. The last box in the MDC Body contains "IND" which means "Indicate" and refers to a visual display on the CRT.

b. Triangle: Each triangle points to a box and means that the signal or voltage the box represents must be available. These signals and voltages are used by the functions (represented by circles) following (or associated with) the triangle.

c. Circle: Each circle represents a functional part of the circuit. When the circle is solid, it represents the entire function. When the circle is half-solid, it represents only a portion of the function. Arrows through a circle mean the function controls something adjustable.

d. Double Arrowheads: These are placed on feedback lines. Notice that the triangles on these lines are inverted so they point to the output of the loop.

The interpretation of these symbols is:



When SS-1 is available and a part of PS-1 is good, then SS-30 will be available. When SS-30 is available, and all of Freq-1 is good, and a part of IC-1 is good, then SS-34 will be available. What parts of PS-1 and IC-1 have been proven good? Only those parts which are necessary to give the output signals on each line. Note that the first line depends on SS-1 and the second line depends on the first line. Since all of Freq-1 has to be good to produce SS-34, its circle was completely filled in. It also implies that Freq-1 has to be somewhere in the proper adjustment range or SS-34 would not be in specification; however, this is not a hard and fast rule.

In the Heading, section c, the shorthand notation such as J106-7/GN means to measure Jack 106, pin 7 with respect to ground.

To test a Monitor:

a. Follow Preliminary Instructions, section a.
b. Follow instructions in the Prodecure Column, section b, one step at a time.
c. During each step, check voltage and signal availabilities per the Signal Specifications, section g.
d. Locate faulty components by finding the last good signal or voltage prior to a signal or voltage which is not good. Faulty components between these two points can then be isolated by standard testing procedures, including replacement of a suspected component.
e. Feedback lines depend on output Lines, which (in turn) depend on feedback lines. If trouble has been isolated to a feedback loop, break the loop and use standard testing procedures to isolate faulty component(s).

WARNING

All Signal Specification Numbers in heavily outlined boxes indicate signals or voltages of 70 or more volts.